UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,979	01/02/2004	Dong-Ho Lee	9903-074	5476

20575 7590 01/18/2006

MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/750,979	LEE, DONG-HO
	Examiner	Art Unit
	Thao X. Le	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-13 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-13 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 21 Dec. 2005 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

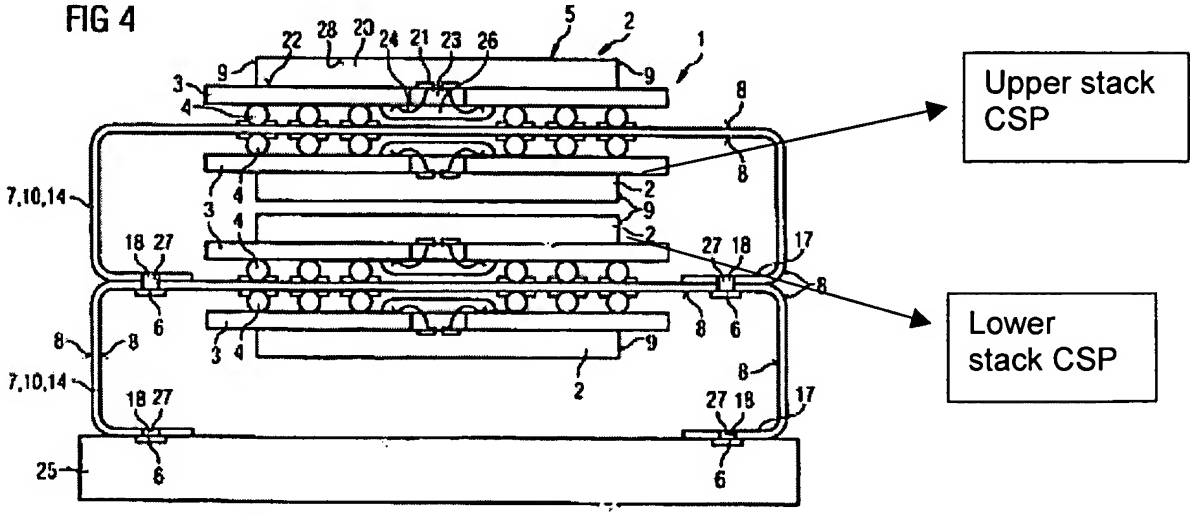
> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3-5, 8-13, and 21-26 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6768191 to Wennemuth et al.

Regarding claim 1, Wennemuth discloses in fig. 4 a stack package including two or more area array type chip scale packages (20/3), each chip scale package comprising: a substrate 3, col. 10 line 4, a plurality of ball land pads 4, col. 10 line 11,

formed on a lower surface of the substrate 3, a plurality of circuit patterns (rewiring line), col. 10 line 11, formed on the lower surface of the substrate 3 and electrically connected to the ball land pads 4 (each of ball comprises a land pad for making contact), fig. 4; and one or more chips 20, col. 10 line 5, installed on an upper surface of the substrate 3 and electrically connected to the circuit patterns, wherein each chip scale package of an adjacent pair of chip scale packages is attached to the other in a manner where the ball land pads 4 of the upper stacked chip scale package face in the opposite direction as the ball land pads 4 of the lower stacked chip scale packages, and wherein the circuit patterns on the lower surface of the substrate of the upper stacked chip scale package are electrically connected to those the circuit pattern 4 on the lower surface of the substrate of the lower stacked chip scale package, fig. 4, by connecting board 8, col. 10 line 21, to the circuit pattern on the lower surface of the substrate on the upper stacked chip and the circuit pattern on the lower surface of the substrate of the lower staked chip.

FIG 4



Regarding claims 3-5, Wennemuth discloses the stack package wherein each connecting board comprises a flexible film 7, col. 10 lines 31-32, and wiring patterns 8, col. 10 line 17, formed on the film 7, wherein a hole 23, col. 10 line 6, is formed in the substrate 3 of each chip scale package, and the chip is electrically connected to the circuit patterns by bonding wires 24, col. 10 line 10, passing through the hole 23, fig. 4, wherein a plurality of bonding pads 21, col. 10 line 8, of each chip size package are formed on the central region of the chip 20 and exposed through hole 23, and wherein one end of each bonding wire is attached to a corresponding bonding pad of the chip, fig. 4.

Regarding claims 8-10, Wennemuth discloses the stack package wherein a plurality of solder balls 4 is formed on the ball land pads of the lowest stacked chip scale package, fig. 4, wherein a single chip scale package is stacked on, and electrically connected through a plurality of solder balls 4 to adjacent stacked chip scale packages coupled by connecting board 8, fig. 8, wherein an adjacently stacked chip scale packages coupled by connecting boards 8 are stacked on, and electrically connected through a plurality of solder balls 4 to another adjacent stacked chip scale packages coupled by connecting boards, fig. 4.

Regarding claims 11-13, Wennemuth discloses the stack package wherein a plurality of connection pads are formed on the outside of the region of the substrate 3 on which a plurality of ball land pads are formed, and electrically connected to the circuit patterns, fig. 4, wherein connecting boards 8 are connected to the circuit patterns

through the connecting pads 4, wherein both ends of the connecting board at which the connecting board is attached to the connection pad are bent, fig. 4.

Regarding claim 21, Wennemuth discloses a stack package in fig. 4 comprising: a first array type chip scale package (CSP) having a substrate 3, and second array type chip CSP having a substrate, second matrix of ball land pads 4 and one or more chip 20s installed on an upper surface of the substrate, wherein the lower surface of the substrate of CSP face the opposite direction, and wherein the first matrix ball land pads is the same size as the second matrix of ball land pads, fig. 4.

Regarding claim 22, Wennemuth discloses thee stack package, wherein each CSP includes a circuit pattern (substrate 3 includes rewiring), col. 10 line 5, formed on the lower surface of the substrate that is electrically connected to the ball land pads 4, and the circuit patterns on the two chip scale packages are electrically connected, fig. 4.

Regarding claims 23-24, Wennemuth discloses the stack package wherein the circuit patterns on the two chip scale packages are electrically connected by connecting boards 8, wherein the stack package further comprising a plurality of solder balls 4 formed on the ball land pads of the first chip scale package.

Regarding claim 25, Wennemuth discloses the stack package further comprising a third chip scale package having a third matrix of ball land pads 4 the same size as the first and second matrices of ball land pads, wherein the third chip scale package is electrically connected to the ball land pads of the second chip scale package through a plurality of solder balls 4 formed on the third matrix of ball land pads on a lower surface of a substrate of the third chip scale package, fig. 4.

Regarding claim 26, Wennemuth discloses the stack package, further comprising: a third chip scale package having a substrate 3, a third matrix of ball land pads and one or more chips installed on a lower surface of the substrate; and a fourth chip scale package having a substrate 3, a fourth matrix of ball land pads and one or more chips installed on a lower surface of the substrate, wherein the lower surfaces of the substrates of the third and fourth chip scale packages face the opposite direction, wherein the third and fourth matrices of ball land- pads are the same size as the third and second matrices of ball land pads, and wherein the third chip scale package is electrically connected to the ball land pads of the second chip scale package through a plurality of solder balls formed on the third matrix of ball land pads of the third chip scale package, fig. 4.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6768191 to Wennemuth et al in view of US Pub. 2004/0124518 to Karnezos.

Regarding claims 6-7, Wennemuth discloses the stack package wherein the bonding wires 24 are protected by a second encapsulating part 26.

But Wennemuth does not disclose the stack package wherein the chip is protected by a first encapsulating part, and wherein each chip scale package of an adjacent pair of chip scale packages is attached to the other by an adhesive applied on the first encapsulating part.

However, Karnezos discloses the stack package wherein each chip scale package in fig. 10A of an adjacent pair of chip scale packages is attached to the other by an adhesive 1008 applied on the first encapsulating part 1007, fig. 5A or 10 [0191] and [0192]. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of Karnezos with Wennemuth's device because it would have provide the protection as taught by Karnezos [0098].

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
Patent Examiner
08 Jan. 2006